

EXPRESS MAIL MAILING LABEL NO. EV289511768US

PATENT  
Attorney Docket No. ASC-044  
(366/29)

*COPY OF IDS SUBMITTED ON 04/11/03*  
IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT(S): Fitzgerald et al. CONFIRMATION NO.: 2812  
SERIAL NO.: 09/884,172 GROUP NO.: 2822  
FILING DATE: June 19, 2001 EXAMINER: Lattin, C.  
TITLE: Method of Fabricating CMOS Inverter and Integrated Circuits  
Utilizing Strained Silicon Surface Channel MOSFETs

Box RCE  
Commissioner for Patents  
Washington, D.C. 20231

**SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT**

Sir:

In accordance with the provisions of 37 C.F.R. 1.97 and 1.98, Applicants hereby make of record the patents and publications listed on the accompanying Form PTO-1449, and other information contained herein, for consideration by the Examiner in connection with the examination of the above-identified patent application. Copies of the patents and publications are enclosed.

**REMARKS**

In accordance with the provisions of 37 C.F.R. 1.97, this statement is being filed (CHECK ONE):

- ☒ (1) within three (3) months of the **filing date** of a national application other than a continued prosecution application under 37 C.F.R. 1.53(d), or within three (3) months of the **date of entry of the national stage** as set forth in 37 C.F.R. 1.491 in an international application, or before the mailing of the **first Office action** on the merits, or before the mailing of a **first Office action** after the filing of a request for continued examination under 37 C.F.R. 1.114; or
- ☐ (2) after the period defined in (1) but before the mailing date of a **final action** or a **notice of allowance** under 37 C.F.R. 1.311, and
- ☐ the requisite Statement is below, **OR**
- ☐ the requisite fee under 37 C.F.R. 1.17(p), namely \$180.00, is included herein, or
- ☐ (3) after the mailing date of a **final action** or **notice of allowance** but before the payment of the **issue fee**, **AND**
- ☐ the requisite Statement is below, **AND**

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☐ the requisite petition fee under 37 C.F.R. 1.17(p), namely \$180.00 is included herein.

In addition, Applicants wish to inform the Examiner about the following co-pending patent Applications:

U.S. Serial No. 09/859,138, filed on May 16, 2001, by Fitzgerald.

U.S. Serial No. 09/884,172, filed on June 19, 2001, by Fitzgerald et al.

U.S. Serial No. 10/005,274, filed on December 4, 2001, by Fitzgerald et al.

U.S. Serial No. 10/216,085, filed on August 9, 2002, by Fitzgerald.

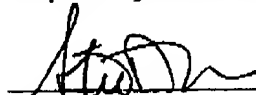
It is respectfully requested that each of the patents and publications listed on the attached Form PTO-1149, and other information contained herein, be made of record in this application.

#### STATEMENT

As required under 37 C.F.R. 1.97(e), Applicant(s), through the undersigned, hereby state either that [check the appropriate space only if either (2) or (3) is checked on the previous page and the Statement is required]:

- ☐ 1. Each item of information contained in the Information Disclosure Statement was first cited in any communication from a foreign patent office in a counterpart foreign application **not more than three months** prior to the filing of the Information Disclosure Statement; or
- ☐ 2. No item of information contained in the Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing this Statement after making reasonable inquiry, no item of information contained in the Information Disclosure Statement was known to **any individual** designated in 37 C.F.R. 1.56(c) **more than three months** prior to the filing of the Information Disclosure Statement.

Respectfully submitted,



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<b>U.S. PATENT DOCUMENTS</b>							
<b>EXAM. INIT.</b>		<b>DOCUMENT NUMBER</b>	<b>DATE</b>	<b>NAME</b>	<b>CLASS</b>	<b>SUB CLASS</b>	<b>FILING DATE IF APPROPRIATE</b>
	A1	US 2002/0140031 A1	10/03/02	Rim	257	347	03/31/01
	A2	US 2002/0125497 A1	09/12/02	Fitzgerald	257	191	07/16/01
	A3	US 2002/0125471 A1	09/12/02	Fitzgerald et al.	257	19	12/04/01
	A4	US 2002/0100942 A1	08/01/01	Fitzgerald et al.	257	369	06/19/01
	A5	US 2001/0003364 A1	06/14/01	Sugawara et al.	257	192	12/08/00
	A6	6,407,406	06/18/2002	Tczuka	257	18	06/29/1999
	A7	6,399,970 B2	06/04/2002	Kubo et al.	257	194	09/16/97
	A8	6,350,993	02/26/02	Chu et al.	257	19	03/12/99
	A9	6,339,232	01/15/02	Takagi	257	192	09/20/99
	A10	6,316,301	11/13/01	Kant	438	197	03/08/00
	A11	6,291,321	08/18/01	Fitzgerald	438	494	03/09/99
	A12	6,266,278	07/24/01	Harari et al.	365	185.18	08/08/00
	A13	6,251,755	06/26/01	Furukawa et al.	438	510	04/22/99
	A14	6,249,022	06/19/01	Lin et al.	257	324	10/22/99
	A15	6,207,977	03/27/01	Augusto	257	192	10/21/98
	A16	6,204,529	03/20/01	Lung et al.	257	314	08/27/99
	A17	6,143,636	11/07/00	Forbes et al.	438	587	08/20/98
	A18	6,130,453	10/10/00	Mei et al.	257	315	01/04/99
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	A20	6,111,267	08/29/00	Fishcher et al.			05/04/98
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	A23	6,058,044	05/02/00	Sugiura et al.	365	185.17	12/09/98
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	A24	5,998,807	12/07/99	Lustig et al.	257	66	09/09/97		
	A25	5,963,817	10/05/99	Chu et al.	438	410	10/16/97		
	A26	5,912,479	06/15/99	Mori et al.	257	192	07/25/97		
	A27	5,891,769	04/06/99	Liaw et al.	438	167	02/27/98		
	A28	5,847,419	12/08/98	Imai et al.	257	192	09/16/97		
	A29	5,792,679	08/11/98	Nakato	438	162	08/30/93		
	A30	5,786,612	07/28/98	Otani et al.	257	316	04/16/96		
	A31	5,739,567	04/14/98	Wong	257	316	11/08/94		
	A32	5,698,869	12/16/97	Yoshim et al.	257	192	09/13/95		
	A33	5,683,934	11/04/97	Candelaria	437	134	05/03/96		
	A34	5,617,351	04/01/97	Bertin et al.	365	185.05	06/05/95		
	A35	5,596,527	01/21/97	Tomioka et al.	365	185.2	02/13/95		
	A36	5,523,592	06/04/96	Nakagawa et al.	257	96	02/01/94		
	A37	5,523,243	06/04/96	Mohammad	437	31	06/08/94		
	A38	5,479,033	12/26/95	Baca et al.	257	192	05/27/94		
	A39	5,461,250	10/24/95	Burghartz et al.	257	347	08/10/92		
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	A41	5,426,316	06/20/95	Mohammad	257	197	06/08/94		
	A42	5,316,958	05/31/94	Meyerson	437	31	05/31/90		
	A43	5,291,439	03/01/94	Kauffmann et al.	365	185	09/12/91		
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<b>FOREIGN PATENT DOCUMENTS</b>									
<b>EXAM. INIT.</b>		<b>DOCUMENT NUMBER</b>	<b>DATE</b>	<b>COUN TRY CODE</b>	<b>CLASS</b>	<b>SUB CLASS</b>	<b>FILING DATE</b>	<b>ABSTR ACT ONLY</b>	<b>ENGLISH LANG (Y/N)</b>
	B1	41 01 167 A1	07/23/92	DE				No	Yes (abstract only)
<b>EXAMINER</b>					<b>DATE CONSIDERED</b>				

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	B2	1 174 928 A1	01/23/02	EP				No	Yes
	B3	1 020 900 A2	07/19/00	EP				No	Yes
	B4	0 683 522 A2	11/22/95	EP				No	Yes
	B5	0 829 908 A2	03/18/98	EP				No	Yes
	B6	0 838 858 A2	04/29/98	EP				No	Yes
	B7	2001319935	05/11/00	JP				Yes	No
	B8	4-307974	10/30/92	JP				No	No
	B9	7-106466	04/21/95	JP				No	No
	B10	11-233744	08/27/99	JP				No	No
	B11	2000-021783	08/31/2000	JP				Yes	Yes
	B12	10-270685	01/29/1999	JP				Yes	Yes
	B13	WO 98/59365	12/30/98	PCT				No	Yes
	B14	WO 00/54338	09/14/00	PCT				No	Yes
	B15	WO 01/54202 A1	07/26/01	PCT				No	Yes
	B16	WO 01/93338 A1	12/06/01	PCT				No	Yes
	B17	WO 01/99169 A2	12/27/01	PCT				No	Yes
	B18	WO 02/15244A2	02/21/02	PCT				No	Yes
	B19	WO 02/13262 A2	02/14/02	PCT				No	Yes
	B20	WO 02/47168 A2	06/13/02	PCT				No	Yes
	B21	WO 02/071488 A1	09/12/02	PCT				No	Yes
	B22	WO 02/071491 A1	09/12/02	PCT				No	Yes
	B23	WO 02/071495 A1	09/12/02	PCT				No	Yes
	B24	WO 99/53539	10/21/99	PCT				No	Yes
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OTHER ART, JOURNAL ARTICLES, ETC.		
EXAM. INIT.	OTHER DOCUMENTS: (Including Author, Title, Date, Relevant Pages, Place of Publication)	
	C1	"2 Bit/Cell EEPROM Cell Using Band to Band Tunneling for Data Read-Out," <u>IBM Technical Disclosure Bulletin</u> , Vol. 35, No. 4B (September 1992) pp. 136-140.
	C2	Armstrong et al., "Design of Si/SiGe Heterojunction Complementary Metal-Oxide-Semiconductor Transistors," <u>IEDM Technical Digest</u> (1995 International Electron Devices Meeting) pp. 761-764.
	C3	Barradas et al., "RBS analysis of MBE-grown SiGe/(001) Si heterostructures with thin, high Ge content SiGe channels for HMOS transistors," <u>Modern Physics Letters B</u> (2001) (abstract).
	C4	Bouillon et al., "Search for the optimal channel architecture for 0.18/0.12 $\mu\text{m}$ bulk CMOS Experimental study," <u>IEEE</u> , (1996) pp. 21.2.1-21.2.4.
	C5	Bufier et al., "Hole transport in strained $\text{Si}_{1-x}\text{Ge}_x$ alloys on $\text{Si}_{1-y}\text{Ge}_y$ substrates," <u>Journal of Applied Physics</u> , Vol. 84, No. 10 (November 15, 1998) pp. 5597-5602.
	C6	Canaperi et al., "Preparation of a relaxed Si-Ge layer on an insulator in fabricating high-speed semiconductor devices with strained epitaxial films," <u>International Business Machines Corporation, USA</u> (2002) (abstract).
	C7	Carlin et al., "High Efficiency GaAs-on-Si Solar Cells with High $V_{oc}$ Using Graded GeSi Buffers," <u>IEEE</u> (2000) pp. 1006-1011
	C8	Cheng et al., "Electron Mobility Enhancement in Strained-Si n-MOSFETs Fabricated on SiGe-on-Insulator (SGOI) Substrates," <u>IEEE Electron Device Letters</u> , Vol. 22, No. 7 (July 2001) pp. 321-323.
	C9	Cheng et al., "Relaxed Silicon-Germanium on Insulator Substrate by Layer Transfer," <u>Journal of Electronic Materials</u> , Vol. 30, No. 12 (2001) pp. L37-L39.
	C10	Cullis et al., "Growth ripples upon strained SiGe epitaxial layers on Si and misfit dislocation interactions," <u>Journal of Vacuum Science and Technology A</u> , Vol. 12, No. 4 (July/August 1994) pp. 1924-1931.
	C11	Currie et al., "Carrier mobilities and process stability of strained S in- and p-MOSFETs on SiGe virtual substrates," <u>J. Vac. Sci. Technol. B</u> , Vol. 19, No. 6 (Nov/Dec 2001) pp. 2268-2279.
	C12	Currie et al., "Controlling threading dislocation densities in Ge on Si using graded SiGe layers and chemical-mechanical polishing," <u>Applied Physics Letters</u> , Vol. 72, No. 14 (April 6, 1998) pp 1718-1720.
	C13	Eaglesham et al., "Dislocation-Free Stranski-Krastanow Growth of Ge on Si(100)," <u>Physical Review Letters</u> , Vol. 64, No. 16 (April 16, 1990) pp. 1943-1946.
	C14	Fischetti et al., "Band structure, deformation potentials, and carrier mobility in strained Si, Ge, and SiGe alloys," <u>J. Appl. Phys.</u> , Vol. 80, No. 4 (August 15, 1996) pp. 2234-2252.
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	<b>C15</b>	Fischetti, "Long-range Coulomb interactions in small Si devices. Part II. Effective electronmobility in thin-oxide structures," <u>Journal of Applied Physics</u> , Vol. 89, No. 2 (January 15, 2001) pp. 1232-1250.
	<b>C16</b>	Fitzgerald et al., "Relaxed $\text{Ge}_x\text{Si}_{1-x}$ structures for III-V integration with Si and high mobility two-dimensional electron gases in Si," <u>J. Vac. Sci. Technol. B</u> , Volume 10, No. 4 (July/August 1992) pp. 1807-1819.
	<b>C17</b>	Fitzgerald et al., "Dislocation dynamics in relaxed graded composition semiconductors," <u>Materials Science and Engineering B67</u> , (1999) pp. 53-61.
	<b>C18</b>	Fitzgerald et al., "Totally relaxed $\text{Ge}_x\text{Si}_{1-x}$ layers with low threading dislocation densities grown on Si substrates," <u>Appl. Phys. Lett.</u> , Vol. 59, No. 7 (August 12, 1991) pp. 811-813.
	<b>C19</b>	Garone et al., "Silicon vapor phase epitaxial growth catalysis by the presence of germane," <u>Applied Physics Letters</u> , Vol. 56, No. 13 (March 26, 1990) pp. 1275-1277.
	<b>C20</b>	Grützmacher et al., "Ge segregation in SiGe/Si heterostructures and its dependence on deposition technique and growth atmosphere," <u>Applied Physics Letters</u> , Vol. 63, No. 18 (November 1, 1993) pp. 2531-2533.
	<b>C21</b>	Hackbarth et al., "Alternatives to thick MBE-grown relaxed SiGe buffers," <u>Thin Solid Films</u> , Vol. 369, (2000) pp. 148-151.
	<b>C22</b>	Hackbarth et al., "Strain relieved SiGe buffers for Si-based heterostructure field-effect transistors," <u>Journal of Crystal Growth</u> , Vol. 201/202 (1999) pp. 734-738.
	<b>C23</b>	Herzog et al., "SiGe-based FETs: buffer issues and device results," <u>Thin Solid Films</u> , Vol. 380 (2000) pp. 36-41.
	<b>C24</b>	Höck et al., "Carrier mobilities in modulation doped $\text{Si}_{1-x}\text{Ge}_x$ heterostructures with respect to FET applications," <u>Thin Solid Films</u> , Vol. 336 (1998) pp. 141-144.
	<b>C25</b>	Höck et al., "High hole mobility in $\text{Si}_{0.17}\text{Ge}_{0.83}$ channel metal-oxide-semiconductor field-effect transistors grown by plasma-enhanced chemical vapor deposition," <u>Applied Physics Letters</u> , Volume 76, No. 26 (June 26, 2000) pp. 3920-3922.
	<b>C26</b>	Höck et al., "High performance 0.25 $\mu\text{m}$ p-type Ge/SiGe MODFETs," <u>Electronics Letters</u> , Vol. 34, No. 19 (September 17, 1998) pp. 1888-1889.
	<b>C27</b>	Ismail et al., "Modulation-doped n-type Si/SiGe with inverted interface," <u>Appl. Phys. Lett.</u> , Vol. 65, No. 10 (September 5, 1994) pp. 1248-1250.
	<b>C28</b>	Kearney et al., "The effect of alloy scattering on the mobility of holes in a $\text{Si}_{1-x}\text{Ge}_x$ quantum well," <u>Semicond. Sci Technol.</u> , Vol. 13 (1998) pp. 174-180.
	<b>C29</b>	Koester et al., "Extremely High Transconductance $\text{Ge/Si}_{0.4}\text{Ge}_{0.6}$ p-MODFET's Grown by UHV-CVD," <u>IEEE Electron Device Letters</u> , Vol. 21, No. 3 (March 2000) pp. 110-112.
	<b>C30</b>	König et al., "Design Rules for n-type SiGe Hetero FETs," <u>Solid-State Electronics</u> , Vol. 41, No. 10 (1997) pp. 1541-1547.
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	<b>C31</b>	König et al., "p-Type Ge-Channel MODFET's with High Transconductance Grown on Si Substrates," <u>IEEE Electron Device Letters</u> , Vol. 14, No. 4 (April 1993) pp. 205-207.
	<b>C32</b>	König et al., "SiGe HBTs and HFETs," <u>Solid-State Electronics</u> , Vol. 38, No. 9 (1995) pp. 1595-1602.
	<b>C33</b>	Lee et al., "Strained Ge channel p-type metal-oxide-semiconductor field-effect transistors grown on Si <sub>1-x</sub> Ge <sub>x</sub> /Si virtual substrates," <u>Applied Physics Letters</u> , Vol. 79, No. 20 (November 12, 2001) pp. 3344-3346.
	<b>C34</b>	Lee et al., "Strained Ge channel p-type MOSFETs fabricated on Si <sub>1-x</sub> Ge <sub>x</sub> /Si virtual substrates," <u>Mat. Res. Soc. Symp. Proc.</u> , Vol. 686 (2002) pp. A1.9.1-A1.9.5.
	<b>C35</b>	Leitz et al., "Channel Engineering of SiGe-Based Heterostructures for High Mobility MOSFETs," <u>Mat. Res. Soc. Symp. Proc.</u> , Vol. 686 (2002) pp. A3.10.1-A3.10.6.
	<b>C36</b>	Leitz et al., "Dislocation glide and blocking kinetics in compositionally graded SiGe/Si," <u>Journal of Applied Physics</u> , Vol. 90, No. 6 (September 15, 2001) pp. 2730-2736.
	<b>C37</b>	Leitz et al., "Hole mobility enhancements in strained Si/Si <sub>1-x</sub> Ge <sub>x</sub> p-type metal-oxide-semiconductor field-effect transistors grown on relaxed Si <sub>1-x</sub> Ge <sub>x</sub> (x<y) virtual substrates," <u>Applied Physics Letters</u> , Vol. 79, No. 25 (December 17, 2001) pp. 4246-4248.
	<b>C38</b>	Li et al., "Design of high speed Si/SiGe heterojunction complementary metal-oxide-semiconductor field effect transistors with reduced short-channel effects," <u>J. Vac. Sci. Technol., A</u> Vol. 20 No.3 (May/June 2002) pp. 1030-1033.
	<b>C39</b>	Maiti et al., "Strained-Si Heterostructure Field Effect Transistors," <u>Semiconductor Science and Technology</u> , Vol. 13 (1998) pp. 1225-1246.
	<b>C40</b>	Meyerson et al., "Cooperative Growth Phenomena in Silicon/Germanium Low-Temperature Epitaxy," <u>Applied Physics Letters</u> , Vol. 53, No. 25 (December 19, 1988) pp. 2555-2557.
	<b>C41</b>	Mizuno et al., "High Performance Strained-Si p-MOSFETs on SiGe-on-Insulator Substrates Fabricated by SIMOX Technology," <u>IEEE IEDM Technical Digest</u> , (1999 International Electron Device Meeting) pp. 934-936.
	<b>C42</b>	Mizuno, "Advanced SOI-MOSFETs with Strained-Si Channel for High Speed CMOS - Electron/Hole Mobility Enhancement" 2000 Symposium on VLSI Technology, Digest of Technical Papers, Honolulu (June 13-15 2000), IEEE NY, NY, pp. 210-211.
	<b>C43</b>	O'Neill et al., "SiGe Virtual substrate N-channel heterojunction MOSFETs," <u>Semicond. Sci. Technol.</u> , Vol. 14 (1999) pp. 784-789.
	<b>C44</b>	Parker et al., "SiGe heterostructure CMOS circuits and applications," <u>Solid State Electronics</u> , Vol. 43 (1999) pp. 1497-1506.
	<b>C45</b>	Ransom et al., "Gate-Self-Aligned n-channel and p-channel Germanium MOSFET's," <u>IEEE Transactions on Electron Devices</u> , Vol. 38, No. 12 (December 1991) pp. 2695.
	<b>C46</b>	Reinking et al., "Fabrication of high-mobility Ge p-channel MOSFETs on Si substrates," <u>Electronics Letters</u> , Vol. 35, No. 6 (March 18, 1999) pp. 503-504.
	<b>C47</b>	Robbins et al., "A model for heterogeneous growth of Si <sub>1-x</sub> Ge <sub>x</sub> films for hydrides," <u>Journal of Applied Physics</u> , Vol. 69, No. 6 (March 15, 1991) pp. 3729-3732.
<b>EXAMINER</b>		<b>DATE CONSIDERED</b>